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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,059	06/24/2003	Charles N. Perez	BUR920030032US1	1058

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EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,059	PEREZ ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/21/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,13,15-17,25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,13,15-17,25,and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication Applicant's Amendment filed 09/21/2005, claims 1, 3-5, 13, 15-17, 25, and 27-29 are pending.

Claims 2, 6-12, 14, 18-24, and 26 have been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-5, 13, 15-17, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (Ma) (US 6,509,622) in view of Kishida et al. (Kishida) (US 2001/0053948).

4. **With respect to claims 1, 13 and 25**, Ma discloses a guard ring within hierarchical integrated circuit design (Ma, col. 3, ll. 29-46, -- a plurality guard ring formed on and coplanar with a plurality metallization levels of an integrated circuit -- and col. 5, ll. 33-65) having a logic design comprising:

Determining (-- establishing --) positions (located) of said logic devices within said integrated circuit design (Ma, col. 2, ll. 55-60 and col. 3, ll. 20-28, -- as figure 1, circuit area 107 is located on die 103 and generally surrounded or encircled by guard ring structure –);

Incorporating (forming) said guard ring into said integrated circuit design (Ma, col. 3, ll. 29-46); and

logic devices (-- portion --) and guard ring symbolically comprise a parameterized symbol (col. 2, ll. 20-29 – type of circuit or device logic such as analog, digital, and mixed signal circuit --; col. 2, ll. 55-60, -- type of guard ring associated with area of electronic devices --, col. 3, ll. 46-67, col. 4, and col. 5, ll. 1-32, -- guard ring efficiency, such as width, thickness, depth and the electrical characteristics --).

Ma does disclose a guard ring within an (-- a hierarchical --) integrated circuit (as per figures 1-4, col. 3, ll. 29-46), which is associated with computer system and program of instructions at least suggest as figure 1-4, but Ma does not specifically detailed of displaying a guard ring within an integrated circuit by using a program of instructions executable by machine.

Kishida discloses specifically in detail of displaying a guard ring in circuit layout (Kishida, fig. 7, guard rings 88 and 90, pg. 3, ¶ 61, ll. 1-8).

Furthermore, Kishida disclose a program storage device readable machine, tangibly embodying a program of instructions executable by the machine to perform a displaying a guard ring within an integrated circuit (Kishida, figures 4 and 5; and page 1, ¶ 4-6).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kishida and Ma references for implementing a method and program of instructions executable by the machine for displaying a circuit design layout includes a guard ring within an integrated circuit with symbolically parameter, that provides user a whole image can easily be obtained the initial stage of layout and thus a layout is edited easily and more efficiently (Kishida, page 2, ¶ 32).

5. **With respect to claims 3-4, 15-16, and 27-28**, Ma and Kishida disclose all the limitations in set forth claims.

Wherein said displaying of said parameterized symbol displays parameters including the type of circuit (Ma, col. 2, ll. 20-29 – type of circuit or device logic such as analog, digital, and mixed signal circuit --); type of guard ring (Ma, col. 2, ll. 55-60, -- type of guard ring associated with area of electronic devices --); and the efficiency of guard ring (col. 3, ll. 46-67, col. 4, and col. 5, ll. 1-32, -- guard ring efficiency, such as width, thickness, depth and the electrical characteristics --).

6. **With respect to claims 5, 17, and 29**, Ma and Kishida disclose all the limitations in set forth claims.

Wherein said displaying of said logic devices (portion) displays and said guard ring graphically comprise illustrating relative position of said logic device and guard ring (Ma, figure 1-4 and the descriptions and col. 3, ll. 20-28).

Response to Arguments

7. Applicant's arguments, filed 09/21/2005, with respect to specification amended have been fully considered and are persuasive. The objection of specification has been withdrawn.

8. Applicant's arguments with respect to claims 1, 3-5, 13, 15-17, 25, and 27-29 have been considered but are moot in view of the new ground(s) of rejection.

In the remarks section on page 8, Applicant argues in substance:

A: Salling does not disclose displaying guard ring(s) within a hierarchical integrated circuit design.

Examiner respectfully considered and moot in view of Ma et al. as the new ground of rejection:

As to A: Ma does disclose displaying guard ring(s) within a hierarchical integrated circuit design (Ma, col. 3, ll. 29-46, -- a plurality guard ring formed on and coplanar with a plurality metallization levels (hierarchical) of an integrated circuit -- and col. 5, ll. 33-65).

In the remarks section on page 10, Applicant argues in substance:

B: Salling does not disclose parameterized symbol or the display of any type of symbol(s).

Examiner respectfully considered and moot in view of Ma et al. as the new ground of rejection:

As to B: Ma does disclose a displaying parameterized symbols (Ma, col. 2, ll. 20-29 – type of circuit or device logic such as analog, digital, and mixed signal circuit --; Ma, col. 2, ll. 55-60, type of guard ring associated with area of electronic devices --, Ma, col. 3, ll. 46-67, col. 4, and col. 5, ll. 1-32, -- guard ring efficiency, such as width, thickness, depth and the electrical characteristics --).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Patent Examiner
Nghia Doan
AU 2825
NMD

VUTHE SIEK
PRIMARY EXAMINER